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EXAMINER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL
BOARD

Ex parte NILS GRAEF and ERICH F. HARATSCH

Appeal 2016-005934
Application 13/510,980
Technology Center 2100

Before JOHN A. JEFFERY, THU A. DANG, and ERIC S. FRAHM,
Administrative Patent Judges.

FRAHM, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

Introduction

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 3, 4, 6–18, 20–23, 25–43, and 45–50. Claims 1, 2, 5, 19, 24, and 44 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b). We reverse the Examiner's anticipation and obviousness rejections of all pending claims, and enter a new ground of rejection for claim 43.

Exemplary Claims

Claims 38, 43, 45, 48, and 49 are independent claims of varying scope, falling into four categories: (i) claim 38 (redirecting a data value to a general process computer), (ii) claims 45 and 48 (selecting between a data value and a decoded output to be provided to a general process computer), (iii) claim 43 (providing a data value to a general process computer), and (iv) claim 49 (processing a data value using a general process computer based on detection of a predefined trigger condition). Exemplary independent claims 38, 43, 45, and 49 under appeal, with emphasis added, read as follows:

38. A method for processing at least one data value obtained from a memory device, said method comprising:
receiving said at least one data value, wherein the at least one data value is included in a data set;
applying a data decode algorithm to the data set by a decoder to yield a decoded output; and
redirecting said at least one data value to a general purpose processor in place of a corresponding element of the decoded output, wherein said at least one data value is not decoded data.

43. A system for processing at least one data value in a read channel of a memory device, comprising:
a memory; and
at least one *processor*, coupled to the memory, operative to:
receive said at least one data value, wherein the at least one data value is included in a data set;
applying a data decode algorithm to the data set by a decoder to yield a decoded output; and
provide said at least one data value for processing by a general purpose processor.

45. A method for processing information in a read channel, said method comprising:
receiving a data set, wherein the data set includes at least one data value;
applying a data decode algorithm to the data set by a decoder to yield a decoded output; and
selecting between the at least one data value and at least one element of the decoded output to be provided for processing by a general purpose processor.

49. A method for processing at least one data value accessed from a storage medium as part of a data set, said method comprising:
receiving said at least one data value;
applying a data decode algorithm to the data set by a decoder to yield a decoded output;
*detecting one or more predefined trigger conditions; and
based at least in part upon detecting the one or more predefined trigger conditions, processing said at least one data value using a general purpose processor.*

Examiner's Rejections

(1) The Examiner rejected claims 3, 4, 6, 7, 10–17, 23, 25–35, 37–43, and 45–50 as being anticipated under 35 U.S.C. § 102(b) by Kanaoka (US 2008/0040651 A1; published Feb. 14, 2008). Final Act. 2–6.

(2) The Examiner rejected claims 8, 9, 18, 20–22, and 36 as being unpatentable under 35 U.S.C. § 103(a) over Kanaoka and Getman (US 2009/0160978 A1; published June 25, 2009). Final Act. 6–7.

ANALYSIS

We agree with Appellants' contentions that Kanoaka fails to disclose (i) the “redirecting. . .” (claim 38), “providing. . .” (claim 43), and “selecting” and “providing” (claims 45 and 48) limitations recited in claims 38, 43, 45, and 48 (*see* App. Br. 14–21; Reply Br. 2–4); a general purpose

processor that is separate and different from the processor also recited in independent claim 43 (App. Br. 16–17; Reply Br. 3); and (iii) detecting and responding to “predefined trigger conditions” as recited in remaining independent claim 49 (App. Br. 21–23; Reply Br. 4).

Specifically, with regard to independent claims 38, 43, 45, and 48, we agree with Appellants that Kanoaka’s main controller (MPU 5) carries out general overall control of the disk drive (*see* Kanoaka ¶ 59), and not decoding functions as recited in each of the independent claims.

And with regard to remaining independent claim 49, Appellants are correct (Reply Br. 3–4) that the Examiner’s *prima facie* case of anticipation is deficient for failing to even address the “predefined trigger condition” limitation of claim 49 (*see* Final Act. 3), as well as claims 20–23, 25–37, and 50 depending therefrom. Additionally, we do not agree with the Examiner’s determination (Ans. 4) that determining a decoded output position and selecting a point at which to process data is analogous to the predefined trigger condition recited in claim 49, in light of Appellants’ Specification (*see* App. Br. 9–10 citing Spec. ¶¶ 74–76; Fig. 6).

In view of the foregoing, Appellants have established that the Examiner erred in determining that Kanaoka anticipates independent claims 38, 43, 45, 48, and 49. Further, because the Examiner relies on Kanoaka’s MPU 5 as teaching the general purpose processor recited in claims 8, 9, 18, 20–22, and 36 (which depend respectively from independent claims 45 and 49), the Examiner also erred in determining that claims 8, 9, 18, 20–22, and 36 would be obvious in view of Kanoaka combined with Getman.

Accordingly, we do not sustain the Examiner’s §§ 102(b), 103(a) rejections based on Kanaoka.

CONCLUSIONS

(1) Appellants have established that the Examiner erred in rejecting (a) claims 3, 4, 6, 7, 10–17, 23, 25–35, 37–42, and 45–50 as being anticipated under 35 U.S.C. § 102(b) by Kanaoka; and (b) claims 8, 9, 18, 20–22, and 36 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Kanaoka and Getman, because (i) the base reference to Kanaoka fails to disclose teach, or suggest a general purpose processor operating as recited in independent claims 38, 45, 48, and 49, and (ii) Kanaoka fails to teach or suggest detecting and responding to a “predefined trigger condition” as recited in independent claim 49.

(2) Appellants have also established the Examiner erred in rejecting claim 43 as being anticipated under 35 U.S.C. § 102(b) by Kanaoka because the Examiner’s finding that Kanaoka’s MPU 5 is equivalent to both the processor and the general purpose processor recited in claim 43, when taken in light of Appellants’ Specification, Drawings, and Claims as originally filed and as a whole, is in error. Because we find that Kanaoka, viewed in a different manner than by the Examiner in the rejection before us, meets the subject matter arranged as recited in claim 43, we enter a new ground of rejection for claim 43.

DECISION

(1) The Examiner’s rejections of (a) claims 3, 4, 6, 7, 10–17, 23, 25–35, 37–43, and 45–50 as being anticipated under 35 U.S.C. § 102(b) by Kanaoka; and (b) claims 8, 9, 18, 20–22, and 36 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Kanaoka and Getman are reversed.

(2) We enter new grounds of rejections under 37 C.F.R. § 41.50(b) for claim 43 as follows:

NEW GROUND OF REJECTION UNDER 37 C.F.R. § 41.50(b)

Under 37 C.F.R. § 41.50(b), we enter a new ground of rejection under 35 U.S.C. § 102(b) for claim 43.

Claim 43 is rejected under 35 U.S.C. § 102(b) as being anticipated by Kanaoka for the same reasons and based on the same findings made by the Examiner (Final Act. 3; Ans. 3–4), with one exception. We find Kanaoka’s decoding unit 60 to be the equivalent of the recited general purpose processor (as opposed to MPU 5), and Kanaoka’s MPU 5 to be the equivalent of the recited processor.

Specifically, Kanaoka discloses a system (Figs. 1 and 3) for processing (e.g., MPU 5 performs “main control” and read channel 20 “controls reproduction and recording” as described in ¶ 59) at least one data value (user data u) in a read channel 20 of a memory device (magnetic disk device 1) having a memory 6, a processor (MPU 5 and/or read channel 20) coupled to the memory 6 and operative to:

receive said at least one data value (user data u), wherein the at least one data value is included in a data set;

apply a data decode algorithm to the data set by a decoder (any or all of channel app decoder 50, decoding unit 60, ECC decoder, and/or LDPC decoder shown in Figs. 1 and 3) to yield a decoded output; and

provide said at least one data value for processing by a general purpose processor (decoding unit 60). *See generally* ¶¶ 52, 57, 59, and 60.

This decision contains new ground of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides that “[a] new ground of rejection

. . . shall not be considered final for judicial review.” 37 C.F.R. § 41.50(b) also provides that Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claim:

(1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED;

37 C.F.R. § 41.50(b)